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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,955	05/10/2001	Bryan Hornung	10001395-1	6603

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,955	HORNUNG ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: On page 50, line 11; "period" is missing at the end of claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 8, 9, 10, 12, 13, 16, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Dishon et al. (US 4,849,978).

Dishon et al. anticipate claim 1.

Dishon et al. teach a computer system capable of performing backward error recovery, comprising: a memory unit having a plurality of memory locations; and a memory controller configured to maintain a checksum in one of said memory locations, said memory controller further configured to receive a plurality of requests to update said checksum with a plurality of data values, said memory controller configured to combine said checksum to each of said data values and to store each of said data values, said memory controller further configured to retrieve a plurality of said data values in response to a data error and to recover a previous state of a particular memory location by combining each of said retrieved data values to said checksum (figure 2, col. 2, lines 33-51, col. 3, lines 14-19, Dishon et al.).

- Dishon et al. anticipate claim 2.

Dishon et al. teach the system, wherein said memory controller is configured to combine each of said retrieved data values to said checksum by exclusively oring each of said retrieved data values to said checksum (col. 3, lines 32-35, Dishon et al.).

- Dishon et al. anticipate claim 3.

Dishon et al. teach the system, wherein each of said data values represents an exclusive or result between a first data value and a second data value that is replaced in memory by said first data value (col. 4, line 68 – col. 5, line 1, Dishon et al.).

- Dishon et al. anticipate claim 8.

Dishon et al. teach the system, wherein said memory controller is configured to identify a particular memory location in response to said data error and to identify which of said data values to retrieve in response to said data error based on which of said data values are associated with said particular memory location (col. 3, lines 32-37, Dishon et al.).

- Dishon et al. anticipate claim 9.

Dishon et al. teach the system, wherein each of said retrieved data values represents an exclusive or result between a first data value and a second data value that is replaced in said particular memory location by said first data value (col. 4, line 68 – col. 5, line 1, Dishon et al.).

- Dishon et al. anticipate claim 10.

Dishon et al. teach a computer system capable of performing backward error recovery, comprising a plurality of memory units, each of said memory units having a plurality of memory locations; and a plurality of memory controllers configured to store to and retrieve from said memory units, one of said memory controllers configured to maintain, in a checksum memory location, a checksum of a checksum set, the other of said memory controllers configured to receive a plurality of write requests for writing to said checksum set, said other memory controllers, for each of said write requests, configured to store a first data value in one of said memory locations, to retrieve a second data value from said one memory location, to combine said first data value with said second data value thereby forming a combined value, and to transmit said combined value to said one memory controller, wherein said one memory controller is configured to update said checksum memory location with a plurality of combined values formed by said other memory controllers and to store each of said plurality of combined values, (figure 2, col. 3, lines 6-32, col. 4, lines 66 - col. 5, line 6, Dishon et al.) said one memory controller further configured to retrieve said stored plurality of combined values in response to a data error and to combine said retrieved combined values with said checksum (col. 5, lines 7-13, Dishon et al.).

- Dishon et al. anticipate claim 12.

Dishon et al. teach the system, wherein said one memory controller is configured to correlate each said plurality of combined values with an identifier that identifies the memory controller that transmitted the correlated combined value to said one memory controller (figure 2, col. 3, lines 14-19, Dishon et al.).

- Dishon et al. anticipate claim 13.

Dishon et al. teach the system, wherein each of said values retrieved by said one memory controller is correlated with the same identifier, said same identifier identifying a failed memory controller (col. 5, lines 7-13, Dishon et al.).

- Dishon et al. anticipate claim 16.

Dishon et al. teach a method for performing backward error recovery, comprising the steps of: storing a plurality of data values within a checksum set to a plurality of memory locations, said checksum set including a checksum value and a plurality of non-checksum values; updating one of said memory locations with a first value; combining said first value to a second value to form a combined value, said second value stored in said one memory location prior to said updating step; updating said checksum value with said combined value; storing said combined value (figure 2, col. 3, lines 6-32, col. 4, line 66 – col. 5, line 6, Dishon et al.); retrieving said combined value in response to a data error; combining said value retrieved in said retrieving step to said checksum value; and recovering a previous state of said one memory location based on said combining said retrieved value step (col. 5, lines 7-13, Dishon et al.).

- Dishon et al. anticipate claim 17.

Dishon et al. teach the method, wherein said combining said first value step includes the step of exclusively oring said first value with said second value (col. 4, line 66 – col. 5, line 1, Dishon et al.), and wherein said combining said retrieved value step includes the step of exclusively oring said checksum value to said retrieved value (col. 5, lines 7-13, Dishon et al.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 4-7, 11, 14, 15, 18, 19, 20, 21, 22, 23, 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dishon et al. (US 4,849,978) as applied to claim 1 above, and further in view of Watson et al. (US 3,573,851).

As per claim 4, Dishon et al. substantially teach the claimed invention described in claim 1 (as rejected above). However Dishon et al. do not explicitly teach the specific use of the system, further comprising a first stack and a second stack, wherein said memory controller is configured to determine which protection domains are associated with said data values, and wherein said memory controller, in storing said data values, is configured to store in said first stack each of said data values determined by said memory controller to be associated with a first protection domain and to store in said second stack each of said data values determined by said memory controller to be associated with a second protection domain.

Watson et al. in an analogous art teach that memory control 18 provides gating, mapping, and protection of the data within the memory stacks as required (figure 2, col. 4, lines 12-16, Watson et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dishon et al.'s patent with the teachings of Watson et al. by including an additional step of using the system, further comprising a first stack and a second stack, wherein said memory controller is configured to determine which protection domains are associated with said data values, and wherein said memory controller, in storing said data values, is configured to store in said first stack each of said data

values determined by said memory controller to be associated with a first protection domain and to store in said second stack each of said data values determined by said memory controller to be associated with a second protection domain.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to store in different memory stacks data corresponding to different protection features and will provide faster processing of data stored in different stacks.

- As per claim 5, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach data error (col. 3, lines 32-34, Dishon et al.).

Watson et al. teach the system, wherein said memory controller is configured to identify one of said protection domains and to select one of said stacks based on which of said protection domains is identified by said memory controller, and wherein each of said retrieved data values is retrieved from said selected stack (col. 4, lines 14-16, lines 30-33, lines 40-42, Watson et al.).

- As per claim 6, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach the system, wherein the memory controller is configured to correlate each of said data values with a memory controller identifier identifying another memory controller that transmitted the correlated data value (figure 2, col. 3, lines 14-19, Dishon et al.).

- As per claim 7, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach the system; wherein each of said retrieved data values is correlated with a memory controller identifier identifying a failed memory controller (col. 5, lines 7-13, Dishon et al.).

- As per claim 11, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the system, wherein said memory locations within said memory units are assigned to different protection domains, and wherein said one memory controller is configured to determine, in a plurality of determinations, which of said protection domains is associated with each of said combined values, said memory controller further configured to store said plurality of combined values associated with different protection domains in different stacks based on said determinations (figure 2, col. 4, lines 14-16, Watson et al.).

- As per claim 14, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the system, wherein said memory locations within said memory units are assigned to different protection domains, and wherein said one memory controller is further configured to identify protection domains and to retrieve said plurality of retrieved combined values based on said identified protection domain (figure 2, col. 4, lines 14-16, lines 30-33, lines 40-42, Watson et al.).

Dishon et al. the identify domains associated with said data error (col. 3, lines 32-33, Dishon et al.).

- As per claim 15, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the system, wherein each of said retrieved combined values is associated with said identified protection domain (col. 4, lines 14-16, lines 40-42, Watson et al.).

- As per claim 18, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach data error (col. 3, lines 32-33, Dishon et al.).

Watson et al. teach the method further comprising the step of associating with a particular protection domain, wherein the retrieving step is based on said associating step (figure 2, col. 4, lines 14-16, lines 40-42, Watson et al.).

- As per claim 19, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the method, further comprising the step of assigning to a respective protection domain each of said memory locations (figure 2, col. 4, lines 14-16, Watson et al.).

Dishon et al. teach storing one of the non-checksum values (col. 3, lines 27-28, Dishon et al.) and storing the combined values (col. 4, line 66 - col. 5, line 1, Dishon et al.).

- As per claim 20, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach storing the combined value (col. 4, line 66 – col. 5, line 1, Dishon et al.).

Watson et al. teach the method, further comprising the step of selecting a stack based on which protection domain is assigned to said one memory location (figure 2, col. 4, lines 14-16, Watson et al.).

- As per claim 21, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach a method for performing backward error recovery, comprising the steps of: storing a plurality of data values within a checksum set to a plurality of memory locations, said checksum set

including a checksum value and a plurality of non-checksum values (figure 2, col. 3, lines 6-32, Dishon et al.).

Dishon et al. teach storing new non-checksum values to said memory locations; for each of said new non-checksum values stored to one of said memory locations, combining said new non-checksum value with a value previously stored in said one memory location thereby forming a combined value; updating said checksum value with each combined value formed via said combining step; storing into memory each combined value formed via said combining step (col. 4, line 66 – col. 5, line 6, Dishon et al.).

Dishon et al. teach detecting a data error; identifying a protection domain associated with said data error; selecting a plurality of combined values formed in said combining step based on said identifying step; combining each of said selected combined values with said checksum value in response to said data error; and recovering a previous state of one of said memory locations based on said combining each of said selected combined values step (col. 5, lines 7-13, Dishon et al.).

Watson et al. teach assigning said memory locations to different protection domains (figure 2, col. 4, lines 14-16, Watson et al.).

- As per claim 22, Dishon et al. and Watson et al. teach the additional limitations.

Dishon et al. teach the method, wherein said combining steps are exclusive oring steps (col. 4, line 66 – col. 5, line 1, Dishon et al.).

- As per claim 23, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the method, further comprising the step of correlating each said value stored in said storing step with a respective one of said protection domains, wherein each value selected in said selecting step is correlated, via said correlating step, with said identified protection domain (figure 2, col. 4, lines 14-16, Watson et al.).

- As per claim 24, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the method, further comprising the step of respectively correlating each said value stored in said storing step with one of said protection domains, wherein said storing step is based on said correlating step (figure 2, col. 4, lines 14-16, Watson et al.).

- As per claim 25, Dishon et al. and Watson et al. teach the additional limitations.

Watson et al. teach the method, wherein said storing step comprises the step of storing into the same stack each value correlated, via said correlating step, with the same protection domain (figure 2, col. 4, lines 12-16, Watson et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100